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1. (canceled).
2. (currently amended) ~~The detector of Claim 1, comprising~~ A piezoelectric detector, comprising:
a piezoelectric transducer;
a transconductance circuit electrically connected to the transducer, the transconductance circuit
defining a common ground and a signal voltage reference not directly connected to the common
ground; and
a transconductance resistor connected to the gate of a field effect transistor (FET), the
transconductance circuit having no ~~high-impedance~~ operational amplifier with an impedance greater
than 10^7 Ohms.
3. (original) The detector of Claim 2, wherein the transconductance resistor is connected to the
gate through an operational amplifier.
4. (original) The detector of Claim 3, wherein the inverting input of the operational amplifier is
connected to the source of the FET.
5. (original) The detector of Claim 4, wherein the non-inverting input of the operational amplifier
is connected to a signal voltage reference.

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6. (original) The detector of Claim 2, comprising an output resistor connected to the source of the FET.

7. (original) The detector of Claim 6, wherein the output resistor is connected to the FET through a bipolar junction transistor (BJT).

8. (original) The detector of Claim 7, wherein the base of the BJT is connected to the source of the FET.

9. (original) The detector of Claim 2, comprising a shorting capacitor connecting the drain of the FET to the source of the FET.

10. (original) The detector of Claim 2, comprising an output voltage divider connected between the gate of the FET and the source of the FET.

11. (currently amended) ~~In a~~ A transconductance detector circuit including a piezoelectric transducer, a field effect transistor (FET) connected to the transducer for amplifying a signal therefrom, a circuit common ground, and a signal voltage reference node at an AC potential other than ground.

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12. (currently amended) The transconductance detector circuit of Claim 11, comprising a transconductance resistor connected to the gate of the FET, ~~the transconductance detector circuit having no high impedance operational amplifier.~~

13. (original) The transconductance detector circuit of Claim 12, wherein the transconductance resistor is connected to the gate through an operational amplifier.

14. (original) The transconductance detector circuit of Claim 13, wherein the inverting input of the operational amplifier is connected to the source of the FET.

15. (original) The transconductance detector circuit of Claim 14, wherein the non-inverting input of the operational amplifier is connected to a signal voltage reference.

16. (original) The transconductance detector circuit of Claim 12, comprising an output resistor connected to the source of the FET.

17. (original) The transconductance detector circuit of Claim 16, wherein the output resistor is connected to the FET through a bipolar junction transistor (BJT).

18. (original) The transconductance detector circuit of Claim 17, wherein the base of the BJT is connected to the source of the FET.

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19. (original) The transconductance detector circuit of Claim 12, comprising a shorting capacitor connecting the drain of the FET to the source of the FET.

20. (original) The transconductance detector circuit of Claim 12, comprising an output voltage divider connected between the gate of the FET and the source of the FET.

21. (canceled)

22. (currently amended) ~~The circuit of Claim 21, comprising~~ A circuit, comprising:
at least one piezoelectric transducer;
at least one transconductance amplifier circuit receiving, along an electrical path, a signal
from the transducer and processing the signal to produce an output; and
a transconductance resistor connected to the gate of a field effect transistor (FET).

23. (currently amended) The circuit of Claim 22, wherein the transconductance resistor is connected to the gate through an operational amplifier having an impedance of no more than 10^7 Ohms.

24. (original) The circuit of Claim 23, wherein the inverting input of the operational amplifier is connected to the source of the FET.

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25. (original) The circuit of Claim 24, wherein the non-inverting input of the operational amplifier is connected to a signal voltage reference.

26. (original) The circuit of Claim 22, comprising an output resistor connected to the source of the FET.

27. (original) The circuit of Claim 26, wherein the output resistor is connected to the FET through a bipolar junction transistor (BJT).

28. (original) The circuit of Claim 27, wherein the base of the BJT is connected to the source of the FET.

29. (original) The circuit of Claim 22, comprising a shorting capacitor connecting the drain of the FET to the source of the FET.

30. (original) The circuit of Claim 22, comprising an output voltage divider connected between the gate of the FET and the source of the FET.

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